Dual Channel Synchronous Gate Driver for Enhancement Mode GaN Transistors

General Description

uP1966D has a single PWM input which is designed to effectively drive both the high-side and low-side enhancement mode Gallium Nitride(GaN) FETs in a synchronous buck regulator application. The floating high-side driver is capable of operating up to 40V.

The uP1966D integrates an adjustable dead time controller, capable of independently setting both high to low and low to high dead times. These dead times are set via external resistors.

The uP1966D has two separate high current gate outputs for both high and low side GaN devices. The two outputs allow for independent adjustment of GaN MOSFET turn-on and turn-off speeds by adding an impedance in series with the respective gate. It features fast-switching speed and minimum propagation delay facilitating high-frequency operation. The uP1966D can operate up to several MHz depending on the application. This device also supports bias supply input under voltage lockout. The uP1966D comes in a WLCSP 1.6x1.6-12B package which minimizes package inductance.

Features

- ❒ 0.4Ω / 0.7 Ω Pull-Down/Pull-Up Resistance
- ❒ Independent Dead Time Adjustment
- ❒ Adjustable Output for Turn-On/Turn-Off Ability
- ❒ Fast Propagation Delays (15ns, Typical)
- ❒ Fast Rise and Fall Times (8ns/4ns, Typical)
- ❒ CMOS Compatible Input-Logic Threshold (Independent of Supply Voltage)
- ❒ Single 5V Driving Voltage Output
- ❒ Three PWM Input States: High, Low and Hi Z
- ❒ Hi Z Input for DCM operation
- ❒ Under Voltage Lockout for Supply Input
- ❒ WLCSP 1.6x1.6-12B Package
- ❒ RoHS Compliant and Halogen Free
- ❒ Low Charge Injection
- ❒ Fast Switching Time

Applications

- ❒ Synchronous Converters

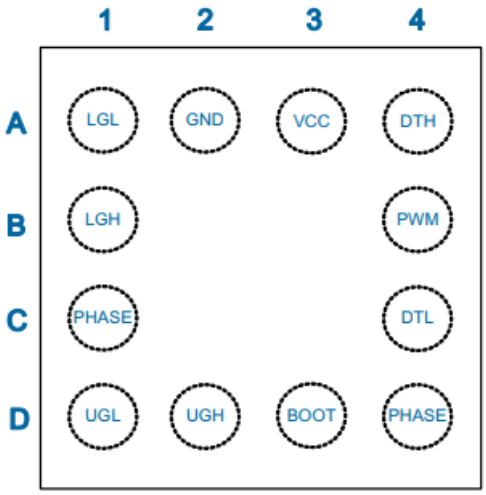
Ordering Information

Order Number	Package	Top Marking
uP1966DFBB	WLCSP1.6x1.6-12B	TBD

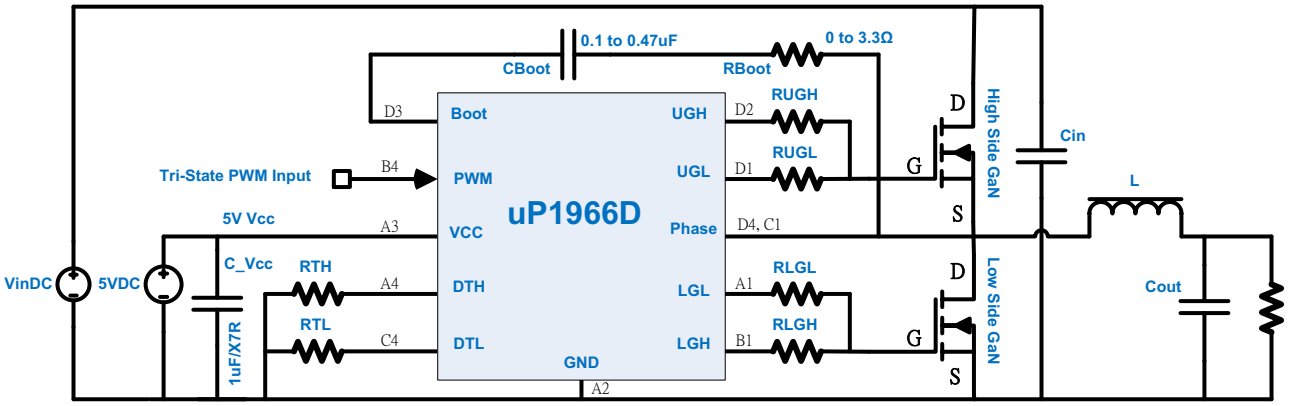
Notes:

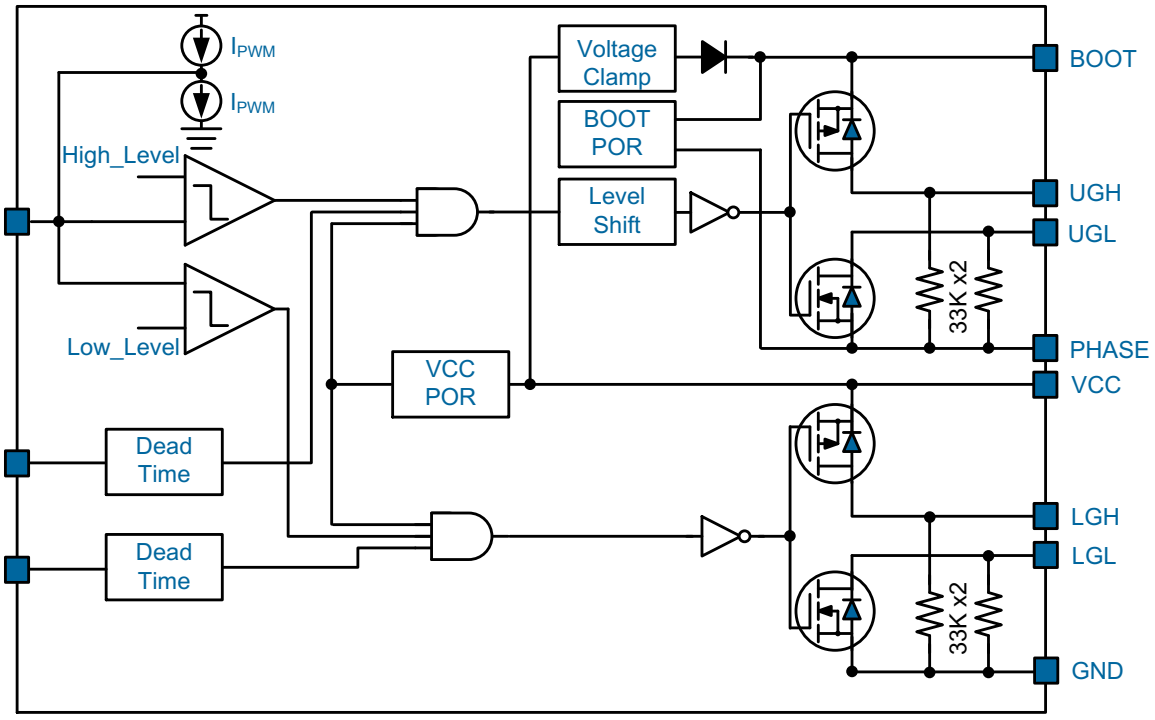
1. Please check the sample/production availability with uPI representatives.
2. uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



Top View





Recommended Operating Conditions[1]

Operating Junction Temperature Range ..... 40ºC to +125ºC
Supply Input Voltage, VCC ..... +4.5V to +5.5V
Power Input Voltage, VIN ..... +4.5V to +40V

Absolute Maximum Ratings[2]

Supply Input Voltage, VCC ..... -0.3V to +7V
BOOT to PHASE ..... -0.3V to +7V
UGH, UGL ..... (PHASE-0.3V) to (BOOT +0.3V)
LGH, LGL ..... -0.3V to (VCC +0.3V)
PWM ..... -0.3V to +7V
DTH, DTL ..... -0.3V to +7V
BOOT to VCC 40V
PHASE to GND 40V
BOOT to GND 45.5V
Storage Temperature Range ..... 55ºC to + 150ºC
Junction Temperature ..... +150ºC
ESD Rating[3]
HBM (Human Body Model) ..... ±2kV

Thermal Information[4]

Package Thermal Resistance

WLCSP 1.6x1.6-12B θ_{JA} 76.8ºC/W
WLCSP 1.6x1.6-12B θ_{JB} 0.6ºC/W
WLCSP 1.6x1.6-12B θ_{JC} 0.65ºC/W

Notes:

1. *The device is not guaranteed to function outside its recommended operating conditions.*
2. *Stresses above Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
3. *Devices are ESD sensitive. Handling precaution recommended.*
4. *θ_{JA} are measured in natural convection at T_A = 25º C on a low thermal conductivity test board using JEDEC 51-3 thermal measurement standard.*

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