15A GaN FET Half-Bridge Power Stage

General Description

The uP9802Q is a fully integrated power stage consisting of a synchronous (half-bridge) driver two 100V GaN FETs of 5.6mΩ (Typ.). A single PWM, tri-state capable, is the only external signal required as dead times, both high-side and low-side turn-on delay, are adjustable via external resistors.

In typical package construction, unlike the uP9802Q, bonding wires are used for interconnections adding both parasitic inductance and resistance. Interconnections within the uP9802Q are accomplished by “flat” low inductance paths. This construction along with the integration of many components that would normally be external such as boot capacitor, boot diode, high-frequency V_{IN} bypass capacitors, and high-frequency V_{CC} bypass capacitors help save PCB space, lower cost, increase robustness and lessen layout criticality and PCB stack-up requirements.

Enhanced electrical characteristics include a UVLO on V_{CC}, short propagation delays, high side low side matching propagation delays, low C_{OSS} GaN FETs, and a Tri-state input which allows DCM operation of synchronous converters. Multi-MHz operation is possible.

Packaged in an ultra-low profile (0.55mm max) PLP 5x6-12L the uP9802Q applies to any non-isolated 48V input synchronous regulator application with outputs up to 15A.

Ordering Information

Order Number	Package	Top Marking
uP9802Q3A1	PLP5X6 -12L	uP9802Q

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

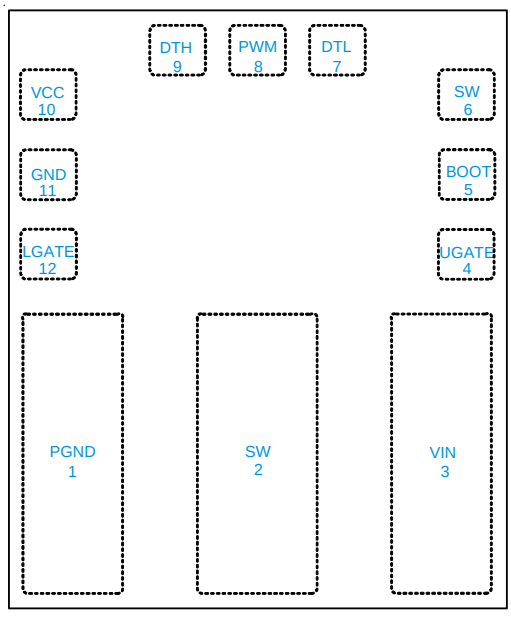
Features

- **Max Input Voltage to 65V DC**
- **Integrated 100V, 5.6mΩ (Typ.) GaN FETs**
- **Internal Bootstrap and VCC Capacitance**
- **Optimized Integrated IC for Parasitic Effect**
- **Individual Dead Time Adjustment**
- **Fast Propagation Delay: 15ns (Typ.)**
- **CMOS Compatible Input-Logic Threshold (Independent of Supply Voltage)**
- **Under Voltage Lockout for VCC Input**
- **Available in PLP5X6-12L Package**
- **RoHS Compliant and Halogen Free**

Applications

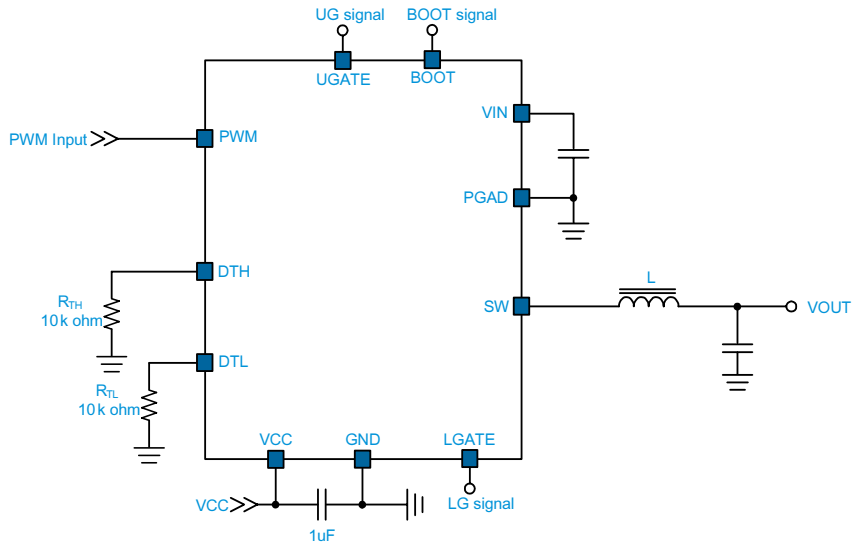
- **Telecom Half and Full Bridge DC-DC Converter**
- **High Current DC-DC Point of Load (POL) Converter**

Pin Configuration

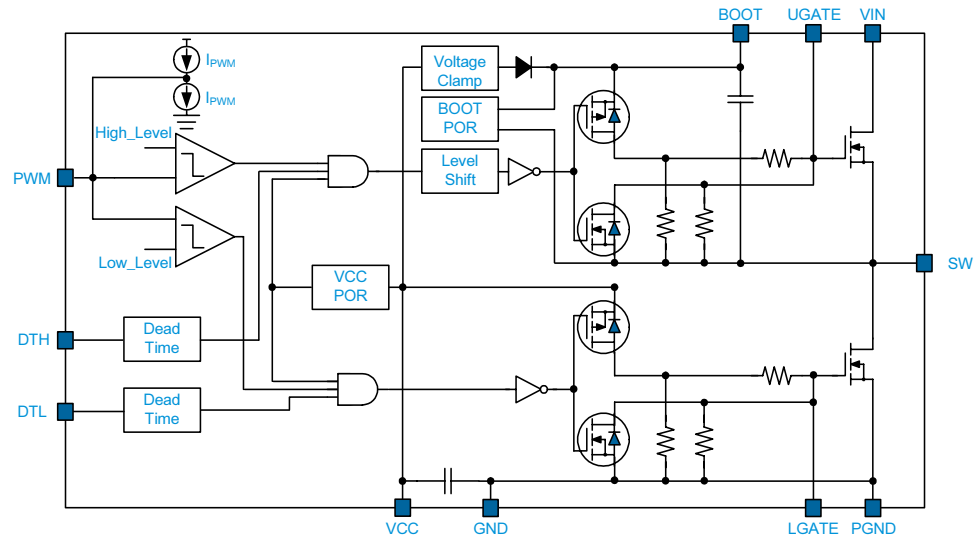


Top View

Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PGND	**Power Ground.** Low side GaN FET source pin. Electrically connect to GND pin.
2.6	SW	**Switch Node.** Half bridge power stage switching node.
3	VIN	**Supply Voltage for the GaN FET.** This pin provides bias voltage for the power stage. Connect this pin to high side drain.
4	UGATE	**Gate Driver Output.** Connect this pin to the gate of high side GaN FET.
5	BOOT	**Bootstrap Supply.** High side gate driver power rail. The bootstrap capacitor C_{BOOT} is internally connected to BOOT pin and SW pin to form a bootstrap circuit.
7	DTL	**Dead Time Control.** Connect this pin to the resistor of ground. Use a resistor to create a dead time between high-side-turn-off and low-side-turn-on.
8	PWM	**PWM Input.** This pin receives logic level input and controls the driver outputs.
9	DTH	**Dead Time Control.** Connect this pin to the resistor of ground. Use a resistor to create a dead time between low-side-turn-off and high-side-turn-on.
10	VCC	**Supply Voltage for the IC.** Thie pin provides bias voltage for the IC. Connect the 5V voltage and to the built-in 1uF MLCC bypass capacitor.
11	GND	**Power Ground for the IC.** All voltage levels are measured with respect to this pin.
12	LGATE	**Gate Driver Output.** Connect this pin to the gate of low side GaN FET.